



# VCAT/LCAS Test Options Datasheet

## Virtual Concatenation/Link Capacity Adjustment Scheme

### PLATFORMS



### MODULES



### KEY FEATURES

#### VCAT Features Include:

- High-Order and Low-Order support
- Insert frame delay or pointer delay on each VCG member
- Supports GFP payload with Ethernet (requires GFP Test Option)

#### LCAS Features Include:

- Automatic and Manual Source and Sink state machine emulation
- Generation of Control Packets
- Monitoring and evaluation of Control Packets
- Plain text State Machine Trace
- Control Packet error generation and detection
- LCAS Protocol Emulation

VCAT (High-Order and Low-Order) and LCAS are separate Test Options for MSA 2030 and NGMR Modules that enable technicians to thoroughly test and troubleshoot today's Next Generation networks.

### VCAT

Test Options are available for High-Order and Low-Order Virtual Concatenation (VCAT).

With either VCAT option or both, the NIC is able to split the SONET/SDH bandwidth into logical groups, called Virtual Concatenation Groups (VCGs) made up of any number of individual elements.

With VCAT, today's networks can leverage existing infrastructure and can significantly increase network utilization by effectively spreading the load across

the whole network. The NIC enables complete testing of VCAT, including the ability to reconfigure the groups on the fly, insert errors and alarms and insert delay in individual members to simulate actual network conditions.

### LCAS

With the Link Capacity Adjustment Scheme (LCAS) Test Option, the NIC can operate to dynamically increase or decrease the bandwidth of VCG groups.

The NIC simulates the on-demand hitless increase or decrease of bandwidth in manual or automatic modes.

The NIC LCAS Test Option enables technicians to fully test and verify LCAS-enabled network equipment and to effectively troubleshoot when required.

# VCAT/LCAS TEST OPTIONS DATASHEET

Virtual Concatenation/Link Capacity Adjustment Scheme

## VCAT SPECIFICATIONS

<b>HO VCAT</b>	STM-64		OC-3	
<b>SDH Mappings</b>	AU-4-VC4-Xv	X = 1 to 24	VT-6-Xv	X = 1 to 21
	AU-3-VC3-Xv	X = 1 to 24	VT-2-Xv	X = 1 to 63
	AU-4-VC3-Xv	X = 1 to 24	VT-1.5-Xv	X = 1 to 64
	STM-16		OC-1	
	AU4-VC4-Xv	X = 1 to 16	VT-6-Xv	X = 1 to 7
	AU3-VC3-Xv	X = 1 to 24	VT-2-Xv	X = 1 to 21
	AU-4-VC3-Xv	X = 1 to 24	VT-1.5-Xv	X = 1 to 28
	STM-4		<i>*Members can be in any available STS-1</i>	
	AU-4-VC4-Xv	X = 1 to 4	<b>Hitless</b>	Per member simultaneous
	AU-3-VC3-Xv	X = 1 to 12	<b>(0 to 256 mS)</b>	
	AU-4-VC3-Xv	X = 1 to 12	<b>Instant</b>	Per member simultaneous
	STM-1		<b>(0 to 256 mS)</b>	
	AU3-VC3-Xv	X = 1 to 3	<b>Payload Patterns</b>	Payload Pattern options common to both High and Low Order mappings: PRBS9 Inv PRBS9 PRBS11 Inv PRBS11 PRBS15 Inv PRBS15 PRBS20 Inv PRBS20 PRBS23 Inv PRBS23 PRBS31 Inv PRBS31 32-Bit User-Defined Pattern
	AU-4-VC3-Xv	X = 1 to 3	<b>GFP Bulk</b>	See GFP and Ethernet data sheets for details
<b>SONET Mappings</b>	OC-192		<b>GFP-F, GFP-T</b>	
	STS-3c-Xv	X = 1 to 24	<b>VCAT</b>	LOA, MSU
	STS-1-Xv	X = 1 to 24	<b>Alarms Detection</b>	LOM Per member simultaneous OOM1 Per member simultaneous OOM2 Per member simultaneous SQM Per member simultaneous
	OC-48		<b>PRBS Payload Error</b>	Bit errors, Loss of pattern sync
	STS-3c-Xv	X = 1 to 16	<b>Alarm Detection</b>	
	STS-1-Xv	X = 1 to 24	<b>VCAT Error/Alarms</b>	Sequence monitoring, and status monitoring is done per member simultaneously
	OC-12		<b>Delay Measure</b>	0 to 256 ms Per member simultaneous
	STS-3c-Xv	X = 1 to 4	<b>Delay Generate</b>	Hitless (0 to 256 mS) Per member simultaneous Instant (0 to 256 mS) Per member simultaneous
	STS-1-Xv	X = 1 to 12	<b>Operations</b>	Change channel #, add channel before selected channel, Delete channel, Delay (ms), Frame Delay, Pointer Delay, Increment Pointer, Hitless Delay (ms), Hitless Frame delay, Hitless Pointer delay, Chane Seq#, Insert LOM, Insert OOM1, Insert OOM2, Sequence Number*
	OC-3		<b>Selectable per VCAT Member</b>	
	STS-1-Xv	X = 1 to 3		<i>*Note: When LCAS is enabled, manual sequence number edit is disabled</i>
<b>LO VCAT</b>	STM-64, STM-16, STM-4		<b>Operations</b>	Delete All, Reset SEQ #s
<b>SDH Mappings*</b>	AU4-TUG3-TUG2-VC2-Xv	X = 1 to 64	<b>Selectable per All Members (VCG)</b>	Clear operations – items form list above
	AU4-TUG3-TUG2-VC12-Xv	X = 1 to 64		
	AU4-TUG3-TUG2-VC11-Xv	X = 1 to 64		
	AU3-TUG2-VC2-Xv	X = 1 to 64		
	AU3-TUG2-VC12-Xv	X = 1 to 64		
	AU3-TUG2-VC11-Xv	X = 1 to 64		
	STM-1			
	AU4-TUG3-TUG2-VC2-Xv	X = 1 to 21		
	AU4-TUG3-TUG2-VC12-Xv	X = 1 to 63		
	AU4-TUG3-TUG2-VC11-Xv	X = 1 to 64		
	AU3-TUG2-VC2-Xv	X = 1 to 21		
	AU3-TUG2-VC12-Xv	X = 1 to 63		
	AU3-TUG2-VC11-Xv	X = 1 to 64		
	STM-0			
	AU3-TUG2-VC2-Xv	X = 1 to 7		
	AU3-TUG2-VC12-Xv	X = 1 to 21		
	AU3-TUG2-VC11-Xv	X = 1 to 28		
	<i>*Members can be in any available AU-3 or Au-4</i>			
<b>SONET Mappings*</b>	OC-192, OC-48, OC-12			
	VT-6-Xv	X = 1 to 64		
	VT-2-Xv	X = 1 to 64		
	VT-1.5-Xv	X = 1 to 64		

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Virtual Concatenation/Link Capacity Adjustment Scheme

## VCAT PARAMETERS

Interface Rate SONET/SDH	Max # of Members Allowed per VCAT Mapping			Max # of Delays per VCAT Member		
	SONET Mapping	SDH Mapping	Max # of (Xv) Members	Maximum Pointer Delays	Maximum Frame Delays	Maximum Combined Delay (ms)
10G OC-192/STM-64	STS-3c-Xv	VC-4-Xv	24	782	2047	255.99984
	STS-1-Xv	VC-3-Xv	24	782*	2047	255.99984
	VT-6-Xv	VC-2-Xv	64	427	511	255.99883
	VT-2-Xv	VC-12-Xv	64	139	511	255.99643
	VT-1.5-Xv	VC-11-Xv	64	103	511	255.99519
2.5G OC-48/STM-16	STS-3c-Xv	VC-4-Xv	16	782	2047	255.99984
	STS-1-Xv	VC-3-Xv	24	782*	2047	255.99984
	VT-6-Xv	VC-2-Xv	64	427	511	255.99883
	VT-2-Xv	VC-12-Xv	64	139	511	255.99643
	VT-1.5-Xv	VC-11-Xv	64	103	511	255.99519
622M OC-12/STM-4	STS-3c-Xv	VC-4-Xv	4	782	2047	255.99984
	STS-1-Xv	VC-3-Xv	12	782*	2047	255.99984
	VT-6-Xv	VC-2-Xv	64	427	511	255.99883
	VT-2-Xv	VC-12-Xv	64	139	511	255.99643
	VT-1.5-Xv	VC-11-Xv	64	103	511	255.99519
155M OC-3/STM-1	STS-1-Xv	VC-3-Xv	3	782*	2047	255.99984
	VT-6-Xv	VC-2-Xv	21	427	511	255.99883
	VT-2-Xv	VC-12-Xv	63	139	511	255.99643
	VT-1.5-Xv	VC-11-Xv	64	103	511	255.99519
52M OC-1/STM-0	VT-6-Xv	VC-2-Xv	7	427	511	255.99883
	VT-2-Xv	VC-12-Xv	21	139	511	255.99643
	VT-1.5-Xv	VC-11-Xv	28	103	511	255.99519

\* (764 for AU-4)

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### LCAS

Complies with the following standards: ITU-T G.707, G.7042, and ANSI T1.105.02-2001.

#### LCAS Feature Description:

Each member of the Tx Virtual Container Group (VCG) is supported by a Source state machine. Each member of the Rx VCG is supported by a Sink state machine. Thus, simultaneous testing of a DUT Source and Sink capability is possible. Automatic mode allows the NIC Source to automatically respond to Sink Member Status (MST) and Re-Sequence Acknowledge (RS-Ack). Similarly, the NIC Sink will respond automatically to received CTRL commands and sequence numbers.

#### LCAS Feature Summary:

- LCAS for High and Low Order VCAT Mappings
- A complete test solution for Low Order LCAS testing including full source and sink functionality
- Supports LCAS Protocol Emulation
- Supports VCAT mappings with a payload type of PRBS, GFP-F, or GFP-T
- Supports from 1 to 63 Low Order or 1 to 24 High Order VCAT members (dependent on interface/mapping configuration)
- Generation of Control Packets
- Supports manual Source and Sink state machine emulation
- Supports the monitoring and evaluation of control packets
- Supports selectable Sink Hold Off and Wait to Restore parameters
- Supports plain text State Machine Trace Logs
- Supports analysis of Source PLCT, TLCT, LOCT, Mo MST, dUMST conditions
- Supports analysis of Sink PLCR, TLCR, LOCR, dSQNC, NON-LCAS conditions
- Supports simultaneous graphical per member Source and Sink results

### LCAS SPECIFICATIONS

**Source State Machine Control (Per Member)** Management command: ADD, ADDN, ALL, REMOVE, REMOVEN, REMOVEALL

**Source State Machine Status (Per Member)** Transmitted Sequence Number; Transmitted Control Word – ADD, NORM, EOS, IDLE, DNU, FIXED; Machine State – IDLE, NORM, DNU, ADD, REMOVE; Received Member Status – OK, FAIL; Active Payload Count, RS-ACK Count, RS-ACK Timeout Count

**Source State Machine Meas. (Per Member)** No MST seconds, dUMST - Persistent unexpected MST count seconds

**Source State Machine Meas. (All Members)** LOCT - Loss of Capacity Transmit seconds  
PLCT - Partial Loss of Capacity Transmit seconds, TLCT - Total Loss of Capacity Transmit seconds

**Sink State Machine Control (All Members)** Sk automatically detects LCAS is being used and configures Sk state

**Sink State Machine Control (Per Members)** Management Command: ADD, ADDN, ADD ALL, REMOVE, REMOVEN, REMOVEALL; Hold off time, wait to restore time

**Sink State Machine Status (Per Member)** RS-Ack count; Active Payload Count; Machine State - OK, FAIL, IDLE; Received Sequence Number; Received Control Field - ADD, NORM, EOS, IDLE, DNU, FIXED

**Sink State Machine Meas. (Per Member)** Non LCAS seconds

**Sink State Machine Meas. (All Members)** LOCR - Loss of Capacity Receive seconds; PLCR - Partial Loss of Capacity Receive seconds; TLCR – Total Loss of Capacity Receive seconds; dSQNC – Inconsistent Sequence Number seconds

**Source and Sink State Machine Trace (All Members)** A state machine trace capability provides the ability to log the state machines state and transitions from state to state in clear text. All state machines or a specific member of the VCG may be traced. This feature allows the verification of the DUT LCAS protocol implementation as well as a debug tool for researching protocol errors.

Each Source trace entry contains the following information:

Member Number; Time stamp; Transmitted Sequence Number; Transmitted Control Field – ADD, NORM, EOS, IDLE, DNU; Source State Machine State – IDLE, NORM, DNU, ADD, REMOVE; Received Member Status – OK, FAIL; Received Re-sequence acknowledge (RS-Ack)

Each Sink trace entry contains the following information:

Member Number; Time stamp; Received Sequence Number; Received Control Field – ADD, NORM, EOS, IDLE, DNU; Sink State Machine State – IDLE, NORM, DNU, ADD, REMOVE; Transmitted Member Status – OK, FAIL; Transmitted Re-sequence acknowledge (RS-Ack)

### ORDERING INFORMATION

Applicable to MSA 2020™, MSA 2030™, ESA 2025™ or NGMR™ modules

- VCAT\_HO\_N - Virtual Concatenation (VCAT) Test Option for High Order Mappings
- VCAT\_LO\_N - Virtual Concatenation (VCAT) Test Option for Low Order Mappings
- LCAS\_N - Link Control Adjustment Scheme (LCAS) Test Option

For more information or a sales quote, visit [www.lightwave.com/contact](http://www.lightwave.com/contact) or email [dlisales@lightwave.com](mailto:dlisales@lightwave.com)



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